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Page 3 Block 46 - After (continued)

THIS CHANGE MUST BE ACCOMPLISHED AFTER: ECP GDMY1238 WHICH RELEASES REVISION D OF THE SPECIFICATION.

NOTE: THIS CR CLOSES WAIVER GDMYW460.

DD Form 1692/C, APR 92

ENGINEERING CHANGE PROPOSAL (ECP), PAGE 2

Form Approved OMB No. 0704-0188

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## **ENGINEERING CHANGE PROPOSAL (ECP), PAGE 3**

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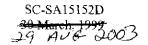
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### 3.5.1.7. Output voltage ripple and noise.

With the maximum load applied across the 5 V and  $\pm$  15 V outputs, the total ripple and noise voltage across the outputs shall not exceed those specified by Table VIII. The ripple voltage shall be the alternating current (AC) voltage component across each output and its return, with a frequency equal to the fundamental switching frequency of the power supply. The noise voltage shall be defined as the AC voltage component across each output and its return with a frequency which is greater than the fundamental switching frequency of the power supply, and shall contain harmonic(s) of fundamental switching frequency and non-harmonic frequency components of the fundamental switching frequency of the power supply. (see 4.8.2.6.2)

Table VIII. Ripple and Noise Outputs

Турс	+5 Vdc Output	± 15 Vdc Outputs
I	250 mV _{pp}	$550~\mathrm{mV_{pp}}$ and $22~\mathrm{mV_{RMS}}$
II	$250~\text{mV}_{\text{pp}}$ and $25~\text{mV}_{\text{RMS}}$	550 mV $_{pp}$ and 22 mV $_{RMS}$

Note: pp = peak-to-peak, RMS = Root Mean Square.

#### 3.5.1.8. Status.

The STATUS signal at pin 7 shall be referenced to the 5 Vdc return (pin 9). A logic "1" signal shall be a voltage level between 2.4 and 5.25 Vdc [including noise and ripple] with a maximum source current of 100 microamperes. The STATUS signal shall have a rise and fall time as specified by Table IX. The rise time is defined as the transition time from 0.6 Vdc to 2.4 Vdc. The STATUS signal line shall be logic "1" at pins 7 (+) and 9 (rtn) when the assembly's output voltages are in the ranges specified in 3.5.1.5 and 3.5.1.6. The STATUS signal line shall be logic "0" at pins 7 (+) and 9 (rtn) when the assembly's output voltage goes into an overvoltage per 3.5.1.11, an undervoltage per 3.5.1.12, or has a short placed across any output to return, separately or in combination per 3.5.1.13. The response time of the status signal shall be 1 ms or less ( $t_{response} < 1$  ms). The response time of the STATUS signal shall be defined as the time interval between a fault (overvoltage, undervoltage, short circuit, etc.) and the STATUS signal falling to a logic "0" (0.0 V to 0.6V) (see 4.8.2.8).

Table IX. Status Signal Response Time

Туре	Input Voltage	Rise/Fall Time (maximum)
I & II	18 to 30 Vdc [inclusive]	90 <del>30</del> μsec
II	14 to 18 Vdc	150 μsec
	30 to 35 Vdc	

Note: Rise/Fall Time =  $\frac{t_{rise}}{t_{fall}}$ 

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across pins 4 and 3 using a measuring device with a minimum bandwidth of 20 MHz. Verify that the measurement is less than or equal to the values specified in 3.5.1.7 for each respective voltage. Measure the RMS ripple and noise voltage across pins 2 and 9 (for Type II only), across pins 8 and 3, and across pins 4 and 3 using a measuring device with a minimum bandwidth of at least three (3) times (3X) the fundamental frequency of the assembly.

[For Type I only] Verify that each measurement is less than or equal to 22 mV_{RMS}.

[For Type II only] Verify that each measurement is less than or equal to 25 mV_{RMS} for the +5 Vdc output only and less than or equal to 22 mV_{RMS} for the +15 Vdc and -15 Vdc outputs.

Note: All verifications shall be performed using a measuring device with 20 MHz bandwidth and all voltage limits include ripple and noise as specified in 3.5.1.8.

4.8.2.8. Status.

4.8.2.8.1. Qualification, first article, control tests.

### 4.8.2.8.1.1. For Types I and II.

Apply a load across pins 2 and 9 capable of providing 3.0  $\pm 0.3$  A of load current. Apply loads across pins 4 and 3 and across pins 8 and 3 capable of providing  $150 \pm 15$  mA of load current each. Place a 24 k $\Omega \pm 1$  percent resistor across pins 7 and 9. Apply the low range of the input voltage as specified in 4.8.2.1 for Type I or Type II, as applicable. Verify that the voltage between pins 7 and 9 is between 2.4 and 5.25 Vdc. Remove the 24 k $\Omega$  resistor across pins 7 and 9 and place a 2.3 k $\Omega \pm 1$  percent resistor from pin 7 to a 5.00  $\pm 0.25$  Vdc external source referenced to pin 9. Place a jumper wire (10  $\Omega$  or less) between pins 2 and 9 and verify that the voltage across pins 7 and 9 is between 0.0 and 0.6 volts. Verify that the fall time from logic "1" and logic "0" is 9030  $\mu$ s. Remove the 2.3 k $\Omega$  resistor and place a 24 k $\Omega \pm 1$  percent resistor across pins 7 and 9. Remove the jumper and verify that the voltage between pins 7 and 9 is between 2.40 and 5.25 Vdc and verify that the rise time from logic "0" and logic "1" is 9030  $\mu$ s or less. Remove the 24 k $\Omega$  resistor across pins 7 and 9 and place a 2.3 k $\Omega \pm 1$  percent resistor from pin 7 to a 5.0  $\pm 0.25$  Vdc external source referenced to pin 9.

Place a jumper wire (10  $\Omega$  or less) between pins 4 and 3. Verify that the voltage between pins 7 and 9 is between 0.0 and 0.6 volts. Verify that the fall time from logic "1" to logic "0" is 9030  $\mu$ s or less. Remove the 2.3 k $\Omega$  resistor and place a 24 k $\Omega$  ± 1 percent resistor across pins 7 and 9. Remove the jumper and verify the voltage between pins 7 and 9 is between 2.4 and 5.25 Vdc and the rise time from logic "0" to logic "1" is 9030  $\mu$ s or less. Remove the 24 k $\Omega$  resistor across pins 7 and 9 and place a 2.3 k $\Omega$  ± 1 percent resistor from pin 7 to a 5.00 ± 0.25 Vdc external source referenced to pin 9. Place a jumper wire (10  $\Omega$  or less) between pins 8 and 3 and verify that the voltage between pins 7 and 9 is between 0.0 and 0.6 Vdc. Verify that the fall time from logic "1" to logic "0" is 9030  $\mu$ s or less. Remove the 2.3 k $\Omega$  resistor and place a 24 k $\Omega$  ± 1 percent resistor across pins 7 and 9. Remove the jumper and verify the voltage between pins 7 and 9 is between 2.40 and 5.25 Vdc and verify that the rise time from logic "0" to logic "1" is 9030  $\mu$ s or less. Repeat the entire test with the high range of the input voltage as specified in 4.8.2.1 for Type I or Type II, as applicable.

The overvoltage requirement of 3.5.1.8 shall be verified during the tests of 4.8.2.11. The undervoltage requirement of 3.5.1.8 shall be verified during the tests of 4.8.2.12.

Note: All verifications shall be performed using a measuring device with 20 MHz bandwidth and all voltage limits include ripple and noise as specified in 3.5.1.8.

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